REMARKS

Claims 1-61 are cancelled; claims 62, 63 and 68 are amended; and claims 62-74 are pending in the application.

The specification is amended to correct a couple of minor typographical errors recently discovered by Applicant.

Claim 68 is objected for having a typographical error, and is amended herein to correct such typographical error. Applicant therefore requests that the objection to claim 68 be withdrawn in the Examiner's next Action.

The pending claims stand rejected as being unpatentable over Applicant's submitted prior in combination with Pfiester (U.S. Patent No. 4,984,042). Applicant respectfully requests reconsideration of such rejections in light of the amendments presented herein.

Referring initially to claim 62, such is amended. The amended claim recites a method in which a pair of partially-formed adjacent transistor gates are formed over a semiconductor substrate, and are formed to each comprise a lowestmost layer of conductive material. The claim further recites that the lowestmost layer of conductive material of one of the partially-formed transistor gates is a first segment, the lowestmost layer of conductive material of the other partially-formed transistor gate is a second segment, and that there is a third segment of conductive material extending between the partially-formed transistor gates from the first segment to the second segment. Finally, the claim, as amended, recites that there are one or more conductively-doped diffusion regions within the substrate and directly under the third segment, with at least one of the one or

more diffusion regions extending from one of the partially-formed transistor gates to the other of the partially-formed transistor gates.

The subject matter added to claim 62 by amendment is supported by the originally-filed application at, for example, Fig. 7 where a pair of partially-formed transistor gates (30 and 32) are shown to comprise a lowestmost layer of conductive material (16), where a segment of conductive material (segment 100) is shown to extend between the lowestmost layers of conductive material of the adjacent transistor gates, and where one or more diffusion regions are shown formed within the substrate and directly under the third segment (diffusion regions 70 and 71), with at least one of said diffusion regions extending from one of the partially-formed transistor gates to the other of the partially-formed transistor gates.

Amended claim 62 is allowable over the cited references for at least the reason that the references do not show or suggest all of the recited features of the amended claim. Specifically, there is no teaching amongst the cited references for the claim 62 recited third segment of conductive material extending between a pair of partially-formed adjacent transistor gates, in combination with the claim 62 recited one or more conductively-doped diffusion regions within a substrate beneath the third segment, of which at least one of the diffusion regions extends from one of the partially-formed transistor gates to the other of the partially-formed transistor gates.

The Examiner cites Applicant's admitted prior art for showing in, for example, Fig. 2, that it was known to form a pair of partially-formed transistor gates having a segment of conductive material extending between them, and cites Pfiester for showing that it was

known to implant dopant through a segment of conductive material into an underlying substrate. The Examiner contends that it would have be known at the time of Applicant's invention to modify the method shown in Applicant's admitted prior art by implanting dopant through a conductive layer as taught in Pfiester, with the motivation being to provide an improved structure and provide an improved process for forming integrated circuits, by allowing charge accumulated during the implant to be bled off by the conductive layer.

Applicant respectfully submits that the combination of Pfiester with Applicant's admitted prior art does not disclose or suggest all the recited features of amended claim 62, and accordingly the claim is allowable over such combination of references. Specifically, there is no teaching within either Pfiester or Applicant's admitted prior art for forming a conductively-doped diffusion region which extends from one partially-formed transistor to another adjacent partially-formed transistor, and under a conductive layer. Further, Applicant notes that the invention of Pfiester shows isolation regions (42 and 43) adjacent the shown transistor device, and accordingly the conductively-doped diffusion regions formed in Pfiester (33, 36, 25, 37, 34) would not extend from one transistor device to another, but rather would be interrupted by the isolation regions. Thus, the combination of Pfiester with Applicant's admitted prior art does not render obvious the amended claim 62 recited structure having a diffusion region under a segment of conductive material and extending from one partially-formed transistor gate to another partially-formed transistor gate. Amended claim 62 is therefore allowable over the Examiner's cited references, and Applicant respectfully requests such allowance in the Examiner's next Action.

Claims 63-67 depend from claim 62, and are therefore are allowable for at least the reasons discussed above regarding claim 62. Applicant therefore requests formal allowance of claims 62-67 in the Examiner's next Action.

Referring next to claim 68, such recites a semiconductor construction comprising conductive layer having a thin segment between a pair of thicker segments, with one of the thicker segments being under a first gate stack and the other being under a second gate stack. The claim further recites that the gate stacks comprise one or more conductive materials over the thicker segments, and one or more insulative materials over the conductive materials, and that at least one conductively-doped region is within the substrate under the thin segment.

The Examiner contends that claim 68 is rendered obvious by the combination of Applicant's admitted prior art with Pfiester. Specifically, the Examiner notes that Applicant's admitted prior art discloses a construction having a conductive layer with a thin segment between a pair of thicker segments, with such thicker segments being under gate stacks; and that Pfiester discloses that it was known in the art to have a conductively-doped diffusion region beneath a segment of conductive material adjacent a partially-formed gate stack. The Examiner then contends that it would be obvious to combine the teachings of Pfiester with Applicant's admitted prior art to create the claim 68 recited structure in which conductively-doped material is beneath a thin segment of conductive material between partially-formed gate stacks. Applicant's respectfully disagrees, and requests reconsideration.

Applicant notes that the conductive material (17) of Pfiester which is provided adjacent the shown gate stack is of uniform thickness, and is of uniform thickness with conductive material comprised by the gate stack. Applicant further notes that Pfiester does not show any partially-formed transistor device adjacent the shown transistor device. To the extent that any inference can be drawn as to what such adjacent transistor device would look like, it would seem most reasonable to infer that the adjacent device would look identical to the device shown in Pfiester, and accordingly would comprise the conductive material 17 having a uniform thickness relative to that of Pfiester's shown device. Thus, to the extent that anything can be inferred from Pfiester about what a structure would look like having a pair of adjacent transistor devices with a conductive layer extending between them, it would be inferred that the conductive layer would be of uniform thickness between the transistor devices and within the transistor devices. In spite of Applicant's teaching in the admitted prior art that there are reasons for thinning a conductive material between a pair of adjacent devices, it would not be obvious to thin the conductive material between any adjacent devices implied by Pfiester as such would add an additional processing step having no apparent benefit to the constructions of Pfiester. Thus, it is not obvious that the combination of Pfiester with Applicant's admitted prior art would lead a person of ordinary skill in the art to form a construction having the claim 68 recited thin segment of conductive material between thicker segments, together with the recited at least one conductively-doped region under the thin segment.

For at least the reasons discussed above, claim 68 is not rendered obvious by the Examiner's combination of references, and Applicant therefore requests allowance of claim 68 in the Examiner's next Action.

Applicant acknowledges the Examiner's indication that Applicant's admitted prior art is only prior art under §102(e), and accordingly Applicant can remove the admitted prior from consideration under §103 with a statement that the admitted prior art and the claimed invention were, at the time of the invention was made, owned by the same person or subject to an obligation of assignment to the same person. Applicant appreciates the Examiner's consideration in mentioning this possible strategy for overcoming the admitted prior art as a §103 reference. Applicant believes, however, that the claims currently pending in the application are allowable over the cited references for the reasons discussed previously in this response. Applicant would prefer that the record reflect that the pending claims are allowable for the cited references as being non-obvious over the combination of references regardless of whether the admitted prior art is appropriate art under §103.

Claims 62-74 are believed allowable for the reasons presented herein, and Applicant therefore respectfully requests that the Examiner's next Action be a Notice of Allowance formally allowing claims 62-74.

Respectfully submitted,

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